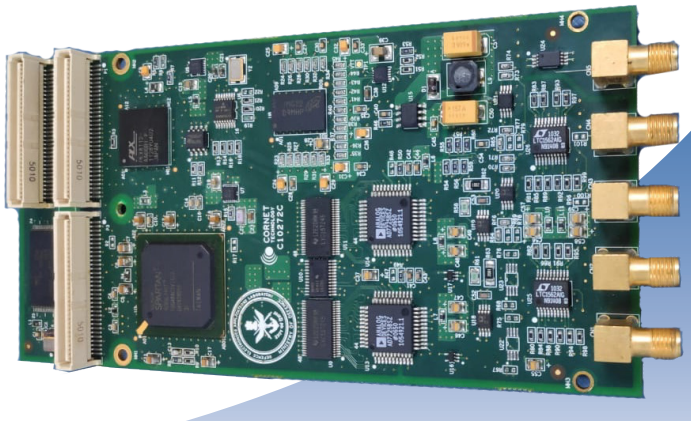
PMC ADC/DAC



Peripheral Component Interconnect Mezzanine Card

(Analog to Digital and Digital to Analog Convertor)

Key Features

- Two Independent 16-bit 500KSPS A/D converters
- ADC input range –
- Two Independent 16-bit 2MSPS D/A converters
- DAC output range-
- 100KHz analog input bandwidth
- Support for under sampling applications
- Xilinx SPARTAN 6 FPGA
- SRAM/SDRAM memory
- Sample clocks: external or on-card PLL
- Software support- Linux/ VxWorks

The ADC/DAC card provides two independent ADC channels and two independent DAC outputs. It integrates two 16-bit ADC channels at 500 KSPS with 100 KHz analog input bandwidth and two 2MSPS 16-bit DAC's with a FPGA for user-code, ample memory for DMA engines and flexible clocks/triggers on a PMC mezzanine format. PCI accessible ADC/DAC buffers.

Each ADC and DAC has independent 16-bit data path to the FPGA. Each can simultaneously read from ADC or write to DAC. The architecture features a high performance front-end tightly coupled to a FPGA. The FPGA communicates with the host processor through a dedicated PCI controller chip, leaving the majority of logic uncommitted. API's for accessing I/O, SRAM/SDRAM, and local bus are provided.

The ADC sample clock is supplied by an on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local crystal oscillator (TCXO) or an external reference can be used to achieve system-wide phase coherence.

The FPGA can be connected to 16-bit QDR SRAM for high speed local data storage. The QDR SRAM provides separate read and write ports to maximize data transfer into and out of memory. This memory can also be used as a high-speed snapshot recorder to store segments of data without interruption from PCI bus traffic

A DMA FPGA core is provided to manage data transfers between the ADC buffer to host memory and host memory to DAC buffer. The DMA engine allows the receiver to automatically initiate a PCI burst transaction when a predetermined number of samples are available. An interrupt is generated by the Channel Adapter when the specified number of data blocks has been written. DMA is interrupt driven.

CORNET TECHNOLOGY

Specifications - (PMC ADC/DAC)

Specifications

PCI IO Bridge:	PLX PCI9056
FPGA:	Xilinx SPARTAN 3S
ADC:	2 Independent Channels
	100 kHz Bandwidth
	Sampling Rate up to 500 kSPS
	16 bit Resolution
DAC :	2 Independent Channels
	100 kHz Bandwidth
	Sampling Rate up to 2 MSPS
	16 bit Resolution
PCI Bus :	PCI 32-bit bus
	33 MHz / 66 MHz
	+3.3V
Front panel :	ADC 2 Channel SMA Connector
	DAC 2 Channel SMA Connector
	Clock SMA connector 3.3V sine wave
JTAG :	FPGA
Rear IO :	IO terminated through PMC P4 connector
Cooling :	Air cooled
Dimension :	149mm x 74mm x 1.6mm
Operating Temperature:	Industrial (–10°C to +55°C)
Voltage :	+3.3 V
Power :	5 Watts on Maximum Conditions
Software :	VxWorks-6.3

Analog Input Characteristics

Channel Count	2 Channels
Channel Config	Differential/Single ended
Acquisition mode	Independent
Resolution	16 Bits
Data Format	2's compliment Binary
Power Consumption	85 (Typ)(mW)
SINAD (dB)	83
SFDR (dB)	94
Input Voltage	+/-2.5V, 50 Ohms bipolar
CMRR	70 dB

Analog Output Characteristics

Channel Count	2 Channels
Channel Config	Single Ended
Output Mode	Independent
Resolution	16 Bits
Data Format	2's compliment Binary
Output Voltage	±2.5V,50 ohms bipolar

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